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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,566	02/23/2004	Bo Jin	10002.003010 (CD03002)	8641

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OKAMOTO & BENEDICTO, LLP
P.O. BOX 641330
SAN JOSE, CA 95164

EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/784,566	JIN ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8-14 and 16-20* is/are rejected.

7)☐ Claim(s) *3,4,7 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~02/04~~ 06/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 3, line 20, modifying "...Application Nos. 10/144,676 and 10/209,088..." to --Application Nos. 10/144,676 now US Patent No. 6,847,218 and 10/209,088 now US Patent No. 6,759,865--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2 and 5-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Cha et al (6849928).

Regarding claim 1, Cha et al disclose an anti-wafer structure [see Fig. 10] for testing a plurality of dice on a wafer under test, the structure comprising a silicon on insulator (SOI) layer (SOI layer 46); and a plurality of probe dice (pad 42) formed on the SOI layer (46), each probe die in the plurality of probe dice having a pad layout corresponding lo a pad layout of a die on the wafer under test.

Regarding claim 2, Cha et al disclose a plurality of holes (holes 34 and 36) extending through the SOI layer (46) and the plurality of probe dice (42), the holes (34 and 36) corresponding to pads (42) on the probe dice.

Regarding claim 5, Cha et al disclose a number of the probe dice (42) equals a number of dice on the wafer under test.

Regarding claim 6, Cha et al disclose the SOI layer (46) comprises an oxide layer (oxide layer 14).

4. Claims 12-14 and 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Cha et al (6849928).

Regarding claim 12, Cha et al disclose [see Fig. 10] a method of fabricating an anti-wafer, comprising providing a substrate (substrate 12), an SOI layer (SOI device 46 and 48) over the substrate (12), and a silicon layer (silicon layer 26) over the SOI layer (46), forming a seal layer (nitride layer 30) over the silicon layer (26); removing the substrate (12), forming an opening (openings 32, 34 and 36) through the SOI layer (46) and the silicon layer (26), and removing the seal layer (30).

Regarding claim 13, Cha et al disclose forming an interconnect line [via opening 32, 34 and 36] extending through the SOI layer (46) and the silicon layer (26).

Regarding claim 14, Cha et al disclose the substrate (12) is removed using a polishing process (CMP polishing).

Regarding claim 16, Cha et al disclose depositing [via chemical vapor deposition CVD] an oxide (oxide layer 28) on the SOI layer (46) after the HF dip process.

Regarding claim 17, Cha et al disclose the seal layer comprises: an oxide layer (oxide layer 28) over the silicon layer (silicon layer 26); and a nitride layer (nitride layer 30) over the oxide layer (28).

Regarding claim18, Cha et al disclose the silicon layer (26) includes pad openings (openings 34 and 36) and the seal layer (30) protects the pad openings (34 and 36) during subsequent processing steps.

Regarding claim 19, Cha et al disclose the SOI layer (46) comprises silicon dioxide (26).

Regarding claim 20, Cha et al disclose the substrate (12) comprises a silicon substrate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al (6759865) in view of Nutty et al (6847218).

Regarding claim 8, Gu et al disclose a probe card (probe card 220) for testing dice (test pads 207) on a wafer under test (wafer 102), the probe card (220) comprising: a tester (101), an anti-wafer (interface 200) having a plurality of probe dice (die pads 203) [see also col. 2, lines

22-23], the anti-wafer (200) having a plurality of interconnect lines (conductive lines 333) extending through holes (holes 334) in the anti-wafer (200), the plurality of interconnect lines (333) coupling pads (207) of the anti-wafer (102) to the board, and an elastomer (interposer 205) located between the anti-wafer (200) and the wafer under test (102), the elastomer (205) providing an electrical connection between pads (207) of the wafer under test (102) and the pads (203) of the anti-wafer (200). However, they do not disclose a board as claimed. Nutty et al disclose a probe card (220) for testing dice on a wafer under test (wafer 102) comprising a board (board 224) for interfacing to a tester (101). Further, Nutty et al teach that the addition of a board is advantageous because it communicates signals from the probe card to the tester. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Gu et al by adding a board to the probe card as taught by Nutty et al in order to communicate signals during testing between the tester and the probe card.

Regarding claim 9, Gu et al disclose a probe card (probe card 220) for testing dice (test pads 207) on a wafer under test (wafer 102). However, they do not disclose a ceramic disk as claimed. Nutty et al disclose a probe card (220) for testing dice on a wafer under test (wafer 102) comprising a ceramic disk (probe substrate 223) [see col. 2, lines 50-51] Further, Nutty et al teach that the addition of a ceramic disk is advantageous because it allows the probe card to be used with commercially available testers and to route cables from a board to a tester interface. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Gu et al by adding a ceramic disk to the probe card as taught by Nutty et al in order to allow a probe card to be used with any commercially available tester and able to route cables from a board to a tester interface.

Regarding claim 10 Gu et al disclose the probe dice (203) are mirror-images of dice (207) on the wafer under test (102).

Regarding claim 11, Nutty et al disclose the board (224) comprises a printed circuit board [see col. 2, line 43].

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Witek et al (6146970), Bolam et al (6563173), Ang (6627484), Seefeldt (6627954), Lin et al (6774395) disclose a method and apparatus for probe card and method of fabrication a probe card.

9. Claims 3-4, 7 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 3, the primary reason for the allowance of the claim is due to an anti-wafer structure comprising holes are filled with interconnect lines coupled to form electrical connections on either side of the anti-wafer structure. Since claim 4 depends from claim 3, it has allowable subject matter.

Regarding claim 7, the primary reason for the allowance of the claim is due to an anti-wafer structure comprising an adapter layer configured to adapt a pad layout of a probe die to another pad layout.

Regarding claim 15, the primary reason for the allowance of the claim is due to a method of fabricating an anti-wafer comprising performing an HF dip process to clean a surface of the SOI layer after the polishing process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Patent Examiner
Art Unit 2829

JMH
March 18, 2005